Future technological innovations will most likely be concentrated on novel materials, structures, or state variables, leading to significant modification of the transistor design. 

**Novel Materials:**
- high-$\alpha$: HfO$_2$, ZrO$_2$, HSICON;
- high-$\mu$: SiGe, III-V, II-VI, CNiTs.

**Novel Structures:**
- multi-gates: double, FinFET, GAA-FET, gate-all-around FET

**Novel State Variables:**
- “Memristance”;
- “Ambipolarity”;

The properties of Si nanowires for Field Effect Transistors are already exploited in the industry to get an improved electrostatic control.

Hence, the planar FET design paradigm is slowly changing to FinFET argue, for whose current drive is a multiple integer of the single nanowire.

An extreme evolution of the FinFET array design is based on vertical stacks of Si nanowire channels. In this case, the current drive is maximized for area density.

### Methods

**Fabricated Structures: a collection**

- **A.** Long nanowire channels with two parallel gate construction.
- **B.** Gate stack cross-section showing three SiNW channels.
- **C.** Optimized Si nanowire precursors before sacrificial oxidation step.
- **D.** A vertical stack of Si nanowire diamonds with 35nmx50nm maximum cross-section.
- **E.** A d=30nm single wire on SOI enclosed in polySi gate together with its SiN mask.
- **F.** A Si Christmas-tree covered by SiO$_2$ and Pt snow.

### Results-I: Circuits with Vertically-Stacked SiNW Arrays [2]

The vertically-stacked Si nanowire (SiNW) top-down technology from device level description to design and implementation of more complex circuits, such as carry-lookahead adders (CLAs).

- **A.** Vertically-stacked inverter structure with SiNW channels anchored to Si pillars with GAA configuration.
- **B.** Evolution of 64 bits CLA-delay with increasing series resistances

### Results-II: Multi-terminal memristive SiNW FETs [3]

New concept of multi-terminal memristive device based on the GAA Schottky barrier field effect transistor concept with Si nanowire (SiNW) channels on bulk-Si wafers has been proposed [3]. In the Figure, I$_d$ vs V$_ds$ characteristic showing the trapping of charges at the metal-semiconductor junction.

### Results-III: Stencilled-gate Schottky-barrier SiNW FETs [4]

Silicon nanowire mechanical switches could be fabricated by means of a simplified process flow. First measurements are promising as high voltage switch applications and Si nanowire resonators.

### Results-IV: High Voltage Mechanical Switches [5]

The large surface to volume ration of SiNWs make these very suitable for biosensing, also in dried environments. In the image a first measurement showing the difference between a functionalized SiNW FET before and after up-take.

### Results-V: Si Nanowire FET for Bio-Detection (in dry env.) [6]

The resistive switching properties of TiO$_2$ layers can be implemented in the BEOL processing. This has been exploited to produce programmable TSV for 3D FPGA architectures with different combinations of top and bottom electrodes.

### Results-VI: TSV-ReRAM for 3D FPGA architectures [7]

Controlled ambipolar I$_d$ vs V$_gs$ characteristics at different V$_gs$ back gate voltages in a double-independent gate ambipolar Si nanowire FET can be exploited to perform several logic operation with a single device.

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### Publications

[8] D. Sacchetto, Y. Leblebici, G. De Micheli, accepted for publication in Electron Device Letters