VERTICALLY-STACKED SILICON NANOWIRE FIELD EFFECT TRANSISTOR ARRAYS

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Process Flow

1- Line pattern  2- DRIE  3- Oxidation  4- Trench fill  5- SiO₂ etch  6- Gate definition

Fabricated Structures

3 SiNWs attached to Si pillars after DRIE
SiNWs embedded in 500nm Poly-Si
Structure after gate-all-around Poly-Si gate patterning

Single SiNW FETs with trapezoidal shape on SOI substrate
Single gate on bent SiNW
Two gates on bent SiNW
Three parallel gates on straight SiNW

Electrical Measurements

References