An Event-Detection High Dynamic Range CMOS Image Sensor

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OUTLINE

- A novel Event-Detection CMOS Image Sensor providing,
- Digital pixel output – lossless readout of the pixel results
- High precision – depends on the counter, dac and comparator results
- High dynamic range – depends on the counter, dac and comparator results
- Low pixel area compared to other digital pixel sensors – reduced pixel level memory

- Characteristics:
  - Pixel level event generation mechanism by using a binary search technique.
  - Technology: UMC 0.18um
  - Photo-active area: p+p-well/p-sub phototransistor
  - (11.24μm × 10.79μm)
  - Total pixel array size: 0-VGA – 160 (H) x 120 (V)
  - Total Pixel Area: 1505.62μm x 4566μm
  - Fill Factor: 34%

- Pixel Mechanism
  - Ramp voltage generation - 10-bit counter + Digital to Analog Converter
  - Clock Analog Comparator: Ramp voltage vs Pixel integrated voltage at each clock cycle
  - Digital Comparison Block: 1 bit memory + XOR
  - pixel previous value vs pixel current value – generation of the event signal

- Similar Designs

PIXEL DESIGN AND TIMING

- Pixel Working Mechanism
  - At the rising edge of Cnt_clk
  - Counter Value – # Vramp decrements
  - When clk_comp = 0
  - if Vramp (Pixel Voltage) > Vramp
  - Comp_out = 1;
  - else
  - Comp_out = 0
  - When clk_done = 1
  - Previous_out = Comp_out;

- Event is generated when Previous_out = Comp_out = 1

PIXEL COMPONENTS

- 5 Transistor SRAM Cell
- COMPARATOR WORKING TIMING

2 STAGE CLOCKED COMPARE

- 1st Stage – Pre-amplifier Stage
- Input: Pixel output (IN) and Ramp voltage (IN-)
- 2nd Stage – Clock comparator:
- Outputs:
  - When CLK = 0
  - OUT1 = 0, OUT2 = 0
  - When CLK = 1
  - if IN- = IN
  - OUT1 = 1, OUT2 = –0
  - else
  - if IN- > IN
  - OUT1 = 0, OUT2 = –1
  - else
  - if IN- < IN
  - OUT1 = 0, OUT2 = –0

PRIORITY ENCODER & COUNTER

- Finite State Machine of the Priority Encoder
- Finite State Machine of the Counter

- Reset: initialized only when receiving a new frame and the counter has decremented to 0:
- IDLE: no event has been found in any pixel and no address has to be registered:
- RUN: single or multiple events have been found and the priority should be shifted and each priority encoder output should be registered which gives the address of the active pixel:
- Hold: only if multiple pixels are active and the priority has to be shifted from one to another until all the active pixel addresses are registered:
- RUN: counter decrements its value at each clock cycle.

TOP LEVEL SCHEMATIC - SIMULATIONS - TOP LEVEL LAYOUT

- SINGLE EVENT GENERATION MECHANISM
- MULTIPLE EVENT GENERATION MECHANISM

Graphs and diagrams showing event detection mechanisms and timing diagrams.