First homogeneous architecture for 3D integrated Multi-Core processor formed by identical KGD chips

ABSTRACT

An innovative modular 3D stacked multi-processor architecture is presented. The platform is composed of identical stacked dies connected together by TSVs. Each die features four 32-bit processors and associated memory modules, interconnected by a 3D NoC, capable of routing packets in the vertical direction. Homogeneous integration minimizes design effort and manufacturing costs, ensuring at the same time high flexibility and re-configurability. Selecting the appropriate number of layers, the platform can target different market segments, being usable as stand alone chip or in 3D stacked fashion. Fully functional samples have been fabricated using a conventional 90nm CMOS process and stacked using a Via-Last Cu-TSV process, developed in-house at EPFL-LSM. Initial results show a target operative frequency of 400 MHz, supporting a vertical data bandwidth of 3.2 Gbps.

3D MODULAR MULTI-CORE ARCHITECTURE

- Increased core count.
- Reduced die area and form factor.
- Improved core to core communication.
- No additional design effort.
- Re-usability of the platform.
- Simple pre-bond testing.
- On chip TSV yield measurements.

COPPER TSVs AND REDUNDANCY LOGIC

- TSVs redundancy:
  - 2 TSVs for data signals;
  - 3 TSVs for Clock, Layer-ID, Reset.

- TSV macro:
  - 4 pads for each signal;
  - ESD protection;
  - Logic for boot test and yield statistics collection.

3D TESTABILITY

- Pre- and post- bonding testability ensured by the homogeneous architecture:
  - JTAG private modules for each Processing Element and Peripheral;
  - JTAG multiplexers interface for debug signals management.
  - Parallel JTAG access to all per-layer cores before stacking directly through I/O pads.
  - Serial JTAG testing (Boundary Scan Chain) to all cores of the 3D system no more directly accessible (bottom layers).

TEST CHIP AND EXPERIMENTAL RESULTS

- Complete 3D system validation on FPGA emulation.
- Pre bond verification on single fabricated dies exploiting:
  - OpenOCD as software debugger;
  - PCBS and FPGA complex setup integrated on a Probe Station.