Diploma Project Presentation

Design of
an Integrated Voltage-Controlled Oscillator in CMOS

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Project Description

- **Settings**
  - Oscillator used in a PLL for CDR
  - 0.18 um standard CMOS technology
  - 4-stage ring oscillator
  - Center frequency 500 MHz

- **Tasks**
  - Study different VCO topologies
  - Evaluate and compare their performances
  - Establish layout for chosen topology
  - Gain design insights for 2.5 GHz VCO

- **Additional problems addressed**
  - Temperature compensation techniques
  - Oscillation amplitude
VCO Specs

- **Frequency**
  - Center frequency: 500 MHz
  - Tuning range: +/- 40%
  - Tuning linearity

- **Amplitude**
  - Output swing: min 400 mV
  - Output load: 50 fF
4-Stage Differential Ring Oscillator

- Inverter chain

\[ \tau \text{: time constant associated with inverter cell} \]
\[ k \text{: small signal gain of inverter cell} \]

- Sustained oscillations

Barkhausen criterion: the system oscillates if the open-loop TF is unity and has zero phase

\[ k = \frac{1}{\cos(\pi/M)} \quad \omega_0 = \frac{\tan(\pi/M)}{\tau} \]

\[ \Rightarrow k = \sqrt{2} \quad \Rightarrow \omega_0 = 1/\tau \]

- Startup condition

a complex-valued pole pair on the right half of the s-plane leads to growing oscillations, which are eventually limited by nonlinear effects

\[ \Rightarrow k \geq \sqrt{2} \]
Basic Delay Cell

- Differential inverter
  - common mode rejection
  - constant current consumption
  - potentially faster

maximal swing:
\[ \Delta V = RI_{SS} \leq \frac{V_{T0}}{n} + V_{DD} \frac{n-1}{n} \]

complete switching:
\[ V_{OV} \leq \frac{\Delta V}{\sqrt{2}} \]

small signal gain:
\[ k = g_{m01}R = \sqrt{\frac{I_{SS}\beta_{01}}{n}}R \]

oscillation frequency:
\[ \tau = RC_{tot} \quad f_0 = \frac{1}{2\pi\tau} \]
\[ f_0 = \frac{\tan(\pi/M)\mu\Delta V}{4\pi\lambda L^2} \]
Oscillation Amplitude: Quasi-Linear Analysis

**general representation**

- Nonlinear Element: $f(x,t)$
- Linear Element: $g(t)$
- Output: $y(t)$

**quasi-linear approximation**

- Quasi-Linear Element: $N(A,s)$
- Linear Element: $G(s)$
- Output: $Y(s)$

Describing function

- $A_x$: $f_0$
- $A_w$: $f_0, 3f_0, 5f_0$
- $A_y$: $f_0, 3f_0, 5f_0$

quasi-linear assumption
Oscillation Amplitude: Describing Function

\[ N(A) = \begin{cases} 
  k & \text{if } |A| \leq E_{sat}/k \\
  \frac{2k}{\pi} \sin^{-1}\left(\frac{E_{sat}}{kA}\right) + \frac{E_{sat}}{kA} \sqrt{1 - \left(\frac{E_{sat}}{kA}\right)^2} & \text{if } |A| > E_{sat}/k 
\end{cases} \]

Barkhausen criterion for M-stage oscillator

\[ N(A) = \frac{1}{\cos(\pi/M)} \]

Theoretical limit

\[ \frac{A_{\text{max}}}{E_{\text{sat}}} = \frac{4}{\pi} \cos\left(\frac{\pi}{M}\right) \]

for a 4-stage oscillator \[ \frac{A_{\text{max}}}{E_{\text{sat}}} = 0.9 \]
Oscillation Amplitude: Experimental Verifications

Amplitude vs. gain

Amplitude vs. Number of stages

Quasi-linear analysis applicable if gain is high and number of stages small
VCO Topologies

Resistance variation

\[ \text{Vin}_a \rightarrow M0 \rightarrow \text{ISS} \rightarrow \text{Vin}_b \]

\[ \text{Vout}_a \rightarrow R \rightarrow \text{Vin}_b \]

\[ \text{Vout}_b \rightarrow R \rightarrow \text{Vout}_a \]

⇒ positive feedback

⇒ replica biasing

Delay interpolation

\[ \text{fast path} \rightarrow \text{slow path} \rightarrow \text{delay interpolation} \]
VCO Topology: Positive Feedback

Delay cell

\[ R = \frac{R_{01}}{1 - g_{m23}R_{01}} \]

\[ f = \frac{1 - g_{m23}R_{01}}{R_{01}C_{tot}} \]

Current steering unit

\[ I_{SS01} + I_{SS23} = \text{const} \]
VCO Topology: Replica Biasing

Replica bias

Delay cell

large signal resistance:

\[ R_{23} = \frac{\Delta V}{I_{SS}} \]

\[ f \approx I_{SS} \]

small signal resistance:

\[ r_{23} = \frac{1}{\beta (V_{DD} - V_{G23} - V_{T0})} \]
VCO Topology: Delay Interpolation

![Diagram of VCO topology]

- **Fast path:**
  \[ T_f = t_{d01} \]

- **Slow path:**
  \[ T_s = t_{d23} + t_{d45} \]

- **Total cell delay**
  \[ T = \alpha_0 T_f + \alpha_1 T_s \quad T_s \approx 2T_f \]
Performance Evaluation & Topology Selection

- Performance comparison

<table>
<thead>
<tr>
<th></th>
<th>positive feedback</th>
<th>delay interpolation</th>
<th>replica biasing</th>
</tr>
</thead>
<tbody>
<tr>
<td>relative tuning range</td>
<td>2.4</td>
<td>1.3</td>
<td>1.5</td>
</tr>
<tr>
<td>power consumption</td>
<td>1.3 mW</td>
<td>1.8 mW</td>
<td>0.66 – 1.1 mW</td>
</tr>
<tr>
<td>area usage</td>
<td>8'912 um²</td>
<td>14'320 um²</td>
<td>6'370 um²</td>
</tr>
<tr>
<td>tuning linearity</td>
<td>good</td>
<td>good</td>
<td>good</td>
</tr>
<tr>
<td>supply pulling</td>
<td>+/- 1%</td>
<td>+/- 1%</td>
<td>+/- 1%</td>
</tr>
</tbody>
</table>

- Main selection criteria
  - flexibility to compensate for temperature and process variations
  - potential operation at 2.5 GHz

Positive Feedback
Phase Stability

- **Leeson Model**
  \[
  L_{\text{total}} \{\Delta f\} = 10 \log \left[ \frac{P_{\text{sideband}}(\omega_0 + \Delta \omega, 1 \text{ Hz})}{P_{\text{carrier}}} \right]
  \]

  \[
  L\{\Delta f\} = \frac{8}{3 \eta} M kT P \left( \frac{V_{\text{DD}}}{V_{\text{char}}} + \frac{V_{\text{DD}}}{R_L I_{\text{tail}}} \right) f_0^2 \Delta f^{-2}
  \]

- **Impulse sensitivity function (ISF)**
  \[
  L\{\Delta f\} \approx \Gamma_rms^2 = \frac{2}{3 \pi} \left( \frac{1}{f'_{\text{max}}} \right)
  \]

  \[
  f_{1/f^3} = f_{1/f} \frac{\Gamma_{\text{dc}}^2}{\Gamma_{\text{rms}}^2}
  \]
Bias Current Compensation Techniques

- Critical factors: frequency and amplitude
- Impact of resistor $R_{01}$ is dominant in temperature and process corners
- Parameters to be held constant:

\[
\Delta V = I_{ss} R_{01} \\
k = \sqrt{\frac{I_{ss} R_{01}^2 \beta_{01}}{n}} \\
R = \frac{R_{01}}{1 - g_{m23} R_{01}} = R_{01} \left(1 + \frac{I_{ss} R_{01}^2 \beta_{23}}{n} + \frac{I_{ss} R_{01}^2 \beta_{23}}{n} + \ldots\right) \\
\Rightarrow I_{ss} R_{01} = \text{const} \\
\Rightarrow I_{ss} R_{01}^2 = \text{const}
\]

- Frequency and amplitude can only be partially compensated

\[I_{ss} \sim 1/R, T\]
Layout Considerations & Floorplan

- Buffered outputs lie on same side (skew minimized)
- Interconnections have same lengths (phase stability)
- All cells have same orientation (good matching)
- Control and supply grids are common to all cells
Frequency Scaling Considerations

- Possible solutions
  - decrease load capacitance by reducing the device dimensions
  - decrease the value of the resistor and increase the bias current

- Limitations
  - channel length
  - tuning range degrades due to short channel effects
  - interconnection parasitics make up a considerable amount of the total parasitics

- Tradeoffs
  - oscillation frequency vs. power consumption
  - tuning range vs. power consumption
Conclusion

- Different topologies studied and simulated at the transistor level
- Detailed design up to layout and verification of selected topology
- Frequency scaling issues discussed
- Different temperature compensation techniques studied and simulated
- Application of quasi-linear analysis to qualitatively explain the amplitude behavior

Improvements:
- Combine positive feedback and replica biasing in order to achieve a more robust design to temperature and process variations
- Apply quasi-linear analysis to explain the amplitude dependance on the oscillation frequency
## Performance Parameters of Final Design

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tuning range</td>
<td>300 – 700 MHz</td>
</tr>
<tr>
<td>Tuning sensitivity</td>
<td>2.1 MHz / mV</td>
</tr>
<tr>
<td>Internal oscillation amplitude</td>
<td>345 mV - 453 mV</td>
</tr>
<tr>
<td>Buffer oscillation amplitude</td>
<td>473 mV – 495 mV</td>
</tr>
<tr>
<td>Tuning linearity</td>
<td>Very good</td>
</tr>
<tr>
<td>Supply pulling</td>
<td>27.5 MHz / V</td>
</tr>
<tr>
<td>Load pulling</td>
<td>- 150 kHz / fF</td>
</tr>
<tr>
<td>Power consumption</td>
<td>5.2 mW</td>
</tr>
<tr>
<td>Area usage</td>
<td>20’000 um²</td>
</tr>
<tr>
<td>Startup time</td>
<td>2.7 ns</td>
</tr>
<tr>
<td>Maximal output load</td>
<td>50 fF</td>
</tr>
<tr>
<td>Harmonic suppression</td>
<td>- 27 dBC</td>
</tr>
</tbody>
</table>
Improvements

- Combination of Replica Biasing & Positive Feedback
Harmonic Attenuation in M-Stage Oscillator

\[ HA_n [\text{dB}] \]

The graph shows the harmonic attenuation \( HA_n \) in dB as a function of the number of stages \( M \). The curves represent different values of \( n \), such as \( n=3 \), \( n=5 \), \( n=7 \), and \( n=9 \). As the number of stages increases, the harmonic attenuation also increases, indicating that the attenuation becomes more significant with more stages.
Frequency & Amplitude vs. Tuning Voltage

oscillation frequency versus tuning voltage

oscillation amplitude versus tuning voltage
Frequency & Amplitude vs. Temperature
Frequency & Amplitude in Resistor Corners

oscillation frequency @ RES corners

oscillation amplitude @ RES corners
Frequency & Amplitude in MOS Corners